1. (Twice Amended) A semiconductor device comprising:

a plurality of semiconductor elements arranged on a substrate; and

a main current electrode which is arranged near said plurality of semiconductor elements and vertically apart from the surface of the substrate, wherein;

each of said plurality of semiconductor elements and said main current electrode are electrically connected, and wherein said main current electrode is arranged above one of said plurality of semiconductor elements or wiring pattern connected to the one of said plurality of semiconductor elements.

7. (Amended) A semiconductor device including one or a plurality of semiconductor elements, comprising :

a substrate on which the one or the plurality of semiconductor elements are arranged;

a case that is arranged in a predetermined position relative to said substrate so that the one of the plurality of semiconductor elements are surrounded; and

a metal member on which a main current electrode of the one of the plurality of semiconductor elements and a terminal for electrically connecting said semiconductor device and a circuit external to said semiconductor device are formed integrally, wherein said metal member is arranged in a position apart from said substrate by using said case without directly contacting said substrate.

REMARKS

Status of the Application

Upon entry of this amendment, claims 1-10 are pending and stand rejected. No new matter has been added to the present application. Applicants note that the Office Action

incorrectly acknowledges the receipt of "some" of the certified copies of priority documents, when "all" documents should have been received. The present application is a National Phase filing, and therefore the standard procedure is for the PCT International Bureau to provide this information to each office. During a telephone conference with the Examiner, attorneys for the Applicants verified that this was the case. Therefore, Applicants respectfully request acknowledgement of the claim for priority.

In view of the foregoing amendments and the following remarks, Applicants respectfully request reconsideration of the present application and an early Notice of Allowance.

Objections of Record

Figures 1 and 2 are objected to under MPEP § 608.02 for not being designated as "Prior Art" because only that which is old is illustrated. Applicants are submitting herewith a "Drawing Change Authorization Request," and a marked-up version of drawing sheets 1 and 2. Entry of the proposed drawing corrections and withdrawal of the drawing objection is earnestly solicited.

Anticipation Rejection – 35 U.S.C. § 102(a)/(b)

Claims 1-6 stand rejected under 35 U.S.C. §102(a)/(b) as allegedly being anticipated by the acknowledged prior art of Figures 1 and 2 of the present application. Applicants respectfully traverse the rejection and request reconsideration because Figures 1 and 2 fail to teach every element of the recited claims.

Applicants respectfully submit that it appears that the Examiner has misidentified the electrode 62 as a main current electrode when this is not the case. *Source electrode 61* of

Figures 1 and 2 of the present application is a main current electrode, so Applicants hereby assume that the Examiner is referring to the source electrode 61 instead of the electrode 62.

Applicants note that Figures 1 and 2 disclose a power module 51 having a plurality of semiconductor elements 57, 58 and a thermal conductor base board 52 attached to the bottom of the power module 51. Source electrode 61 is a main current electrode and is arranged near semiconductor elements 58 and apart from the surface of the substrates 53, 55 and 56. The source electrode 61 is fixed to the thermal conductor base board 52. (*See* application, as filed, page 1, line 16 – page 4, line 10).

In light of the foregoing amendments, Applicants respectfully submit that the Examiner's rejection is moot because the prior art of Figures 1 and 2 does not disclose all of the limitations of newly-amended claim 1. In particular, the prior art of Figures 1 and 2 fails to disclose the claimed "main current electrode [that] is arranged *above* one of said plurality of semiconductor elements or wiring pattern connected to the one of said plurality of semiconductor elements." (Emphasis added). Because the prior art of Figures 1 and 2 do not recite all the limitations of claim 1, Applicants respectfully submit that the prior art of Figures 1 and 2 do not anticipate claim 1. As claims 2-6 ultimately depend from claim 1, Applicants respectfully submit that claims 2-6 are not anticipated by the prior art of Figures 1 and 2, for the reasons set forth above. Withdrawal of the rejection of claims 1-6 is solicited.

Anticipation Rejection – 35 U.S.C. § 102(e)

Claims 7-10 stand rejected under 35 U.S.C. §102(e) as allegedly being anticipated by U.S. Patent No. 6,353,258 (hereinafter "Inoue"). Again, Applicants respectfully traverse the rejection and request reconsideration because Inoue fails to teach every element of the recited claims.

Applicants note that Inoue discloses a semiconductor module having a plurality of power semiconductor devices mounted on a substrate. A metal foil is mounted on the substrate so that an asymmetrical unit arrangement of the semiconductor devices is formed. All units are electrically connected with electrode terminal feet 1601, 1603, 1604 and 1606. The adjustment terminal feet 1604 have a terminal foot 1601 that is *directly connected* to the surface of the substrate as shown in Fig. 15. Thus, in the structure of Inoue, a space for contacting the metal member is required on the surface of the substrate, making difficult any reduction of the size of the semiconductor device. This disadvantage is described at page 3, line 21 through page 4, line 10 of the specification.

In light of the foregoing amendments, Applicants respectfully submit that the Examiner's rejection is moot because Inoue does not disclose all of the limitations of newly-amended claim 1. In particular, Inoue fails to disclose a metal member (which the Examiner equates with the adjustment terminal foot 1604 of Inoue) that is arranged "in a position apart from said substrate by using said case *without directly contacting said substrate.*"

Because Inoue does not recite all the limitations of claim 7, Applicants respectfully submit that Inoue does not anticipate claim 7. As claims 8-10 ultimately depend from claim 7, Applicants respectfully submit that claims 8-10 are not anticipated by Inoue, for the reasons set forth above. Withdrawal of the rejection of claims 7-10 is solicited.

CONCLUSION

In view of the foregoing amendments and remarks, Applicant respectfully submits that the pending claims patentably define over the prior art. Accordingly, a Notice of Allowance is respectfully requested. In the event that the Examiner believes that the present application is not allowable for any reason, the Examiner is encouraged to contact the

undersigned attorney to discuss resolution of any remaining issues.

Date: December 9, 2002

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Please amend the claims to read:

1. (Twice Amended) A semiconductor device comprising:

a plurality of semiconductor elements arranged on a substrate; and

a main current electrode which is arranged near said plurality of semiconductor elements and vertically apart from the surface of the substrate, wherein;

each of said plurality of semiconductor elements and said main current electrode are electrically connected, and wherein said main current electrode is arranged above one of said plurality of semiconductor elements or wiring pattern connected to the one of said plurality of semiconductor elements.

7. (Amended) A semiconductor device including one or a plurality of semiconductor elements, comprising :

a substrate on which the one or the plurality of semiconductor elements are arranged;

a case that is arranged in a predetermined position relative to said substrate so that the one of the plurality of semiconductor elements are surrounded; and

a metal member on which a main current electrode of the one of the plurality of semiconductor elements and a terminal for electrically connecting said semiconductor device and a circuit external to said semiconductor device are formed integrally, wherein said metal member is arranged in a position apart from said substrate by using said case without directly contacting said substrate.